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# Power and Voltage Balance Control of a Novel Three-phase Solid State Transformer Using Multilevel Cascaded H-Bridge Inverters for Microgrid Applications

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***Abstract*—This paper presents a new application of power and voltage balance control schemes for cascaded H-Bridge Multilevel Inverter (CHMI)-based Solid-State Transformer (SST) topology. To reduce load on the controller and simplify modulation algorithm, a master-slave control (MSC) strategy is designed for the dual active bridge (DAB) stage. The master controller executes all control and modulation calculations, and the slave controllers manage only device switching and protection. Due to the inherent power and dc-link voltage unbalance in cascaded H-Bridge based SST, this paper presents a compensation strategy based on three-phase *d-q* decoupled current controller. An optimum zero-sequence component is injected in the modulation scheme so that the three-phase grid currents are balanced. Furthermore, to tightly regulate the output voltage of all the DAB modules to target value a dynamic reference voltage method is also implemented. With this proposed control method the three-phase grid currents and dc-link voltage in each module can be simultaneously balanced. Finally, simulation and experimental results are presented to validate the performance of the controller and its application to microgrid SST.**

***Index Terms*—Cascaded H-bridge Multilevel Inverter (CHMI), Solid-State Transformer (SST), dual active bridge (DAB), three-phase *d-q* decoupled current controller, master-slave control (MSC), power and voltage balance.**

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## I. Introduction

The proliferation of distributed generation and renewable energy resources has motivated the researchers to investigate the feasibility of new microgrid operation mode FREEDM (future renewable electric energy delivery and management system). The FREEDM system is a new medium-voltage microgrid composed of several solid state transformers (SST), high-bandwidth digital communication, and distributed control. As the fundamental component of innovative smart microgrid system, SST is intended to replace the conventional line frequency transformers and performs the power flow control. Conventional transformers possess many undesirable properties including bulky and power quality susceptibility. In contrast, the SST is an intelligent power electronics system with capabilities such as managing power flow, providing power quality improvement and allowing easy connection of the distribution resources[1]-[5].

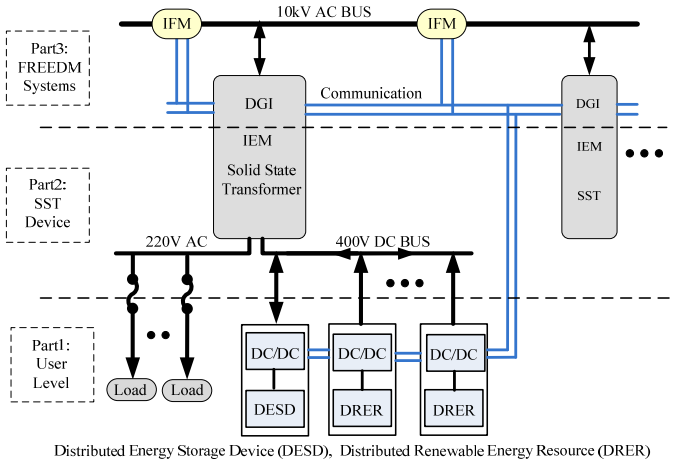


Fig. 1. The microgrid interface of the FREEDM system.

Fig. 1 shows a typical FREEDM system which consists of three parts. The first part is the user level interface that includes both a 400V-dc distribution bus and low voltage 220V-ac bus. The second part is an intelligent energy management (IEM) device, which is connected to 10kV ac distribution bus and supports the regulated buses. The IEM is actually formed by the SST that manages bidirectional power flow control to all devices connected to the low-voltage (400V-dc and 220V-ac) buses and loads. It also has many

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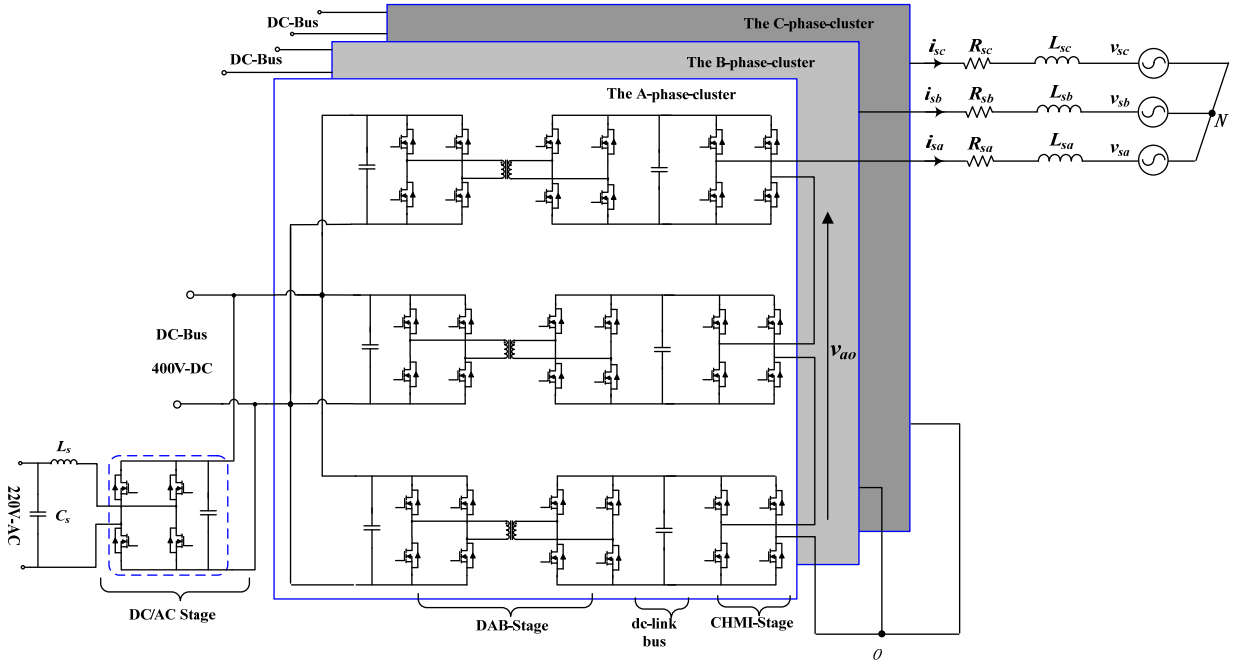


Fig. 2. Topology of the proposed 20kVA three-phase SST.

additional functions such as voltage regulation, voltage sag compensation, fault isolation and harmonic isolation. The third part is called the DGI (Distributed Grid Intelligence) operating system, which is embedded into the IEM device and utilizes the communication network to coordinate the system power management with other energy routers. Furthermore, an intelligent fault management (IFM) device is used to prevent potential faults in the 10kV-ac circuit and reconfiguration capability and uninterrupted power quality to the user [6]-[8].

An important objective of using the SST in the FREEDM system is to achieve compatibility and flexibility. It can regulate the low-voltage buses and provide active and reactive power control or power/frequency control for the grid side port. Fig. 2 shows the proposed 20kVA SST based on the cascaded H-bridge multilevel inverter. The SST consists of a dual active bridge (DAB) dc/dc stage to step up the 400V-dc input to the high-voltage dc link, a cascade H-Bridge multilevel dc/ac inverter stage to provide active power and reactive power for the 10kV-ac grid, and a dc/ac stage to produce a 220V ac residential voltage for loads. In China, the utility systems and residential voltage are 10kV and 220V, respectively.

Despite cascaded H-Bridge topology has been widely used in the SST device because of its modularity to achieve medium-voltage output and good power quality, it also has several drawbacks [9]-[15]. One of the main drawbacks is the power unbalance at different phases and the dc voltage unbalance at different modules. Various configurations for cascaded H-bridge multilevel converter have been reported in [16]-[22], much of previous research mainly focuses on applications in static synchronous compensator (STATCOM), EV traction drive and medium-voltage industrial drives for improving power quality and reliability of a power distribution system. In [20]-[21], the proposed system is implemented based on independent PV solar sources with independent MPPT control algorithm for each PV string. The PV input is connected directly to the cascaded H-Bridge dc/ac module and the dc-dc DAB stage has been eliminated to reduce size of the converter. However, it requires three individual PI controllers for each PV cell to balance the inverter output and there is no isolation between the low and high voltage sides due to the elimination of the DAB stage and its high frequency transformer. A single-phase SST to interface with 7.2kV distribution system has been reported in [22]. It consists of cascaded H-bridge ac–dc rectifier, dc–dc converter (DAB) and ac-dc inverter stages.Through the interaction of the DAB controller with the rectifier controller, the rectifier dc-link voltages and DAB stage powers can be balanced by selecting the voltage feedforward and feedback coefficients in DAB modules. Nevertheless, the optimal selection of these coefficients is not given and it requires 3-indiviual controllers for each DAB module. Furthermore, the power flow from distributed renewable energy source to utility for 3-phase system is not discussed. Different topologies other than DAB dc-dc converter to boost the PV source voltage are also proposed for SST in [23] and [24] but concept is based on transformerless SST where there is no isolation transformer between input and output.

This paper extends some of the control methods developed previously [20]-[22] for different applications and validates the concept by means of numerical simulations, and extensive experimental validation carried out on 10kVA laboratory prototype. The paper investigates the application of the 3-phase SST and its controller with the energy flow from the distributed renewable energy resources to the grid under unbalanced conditions. The control scheme resolve the power and voltage unbalanced problems of 3-phase SST including the unbalanced of different modules (DAB+CHMI) in each phase and finally inject a purely sinusoidal balanced three-phase current into the ac grid. The controller employs the moving floating neutral point control algorithm to balance the power at the three phase ac-side and the dynamic reference voltage method (feedforward compensation) to balance the

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dc-link voltage of different modules in each phase. A master-slave control (MSC) is used to control the output of the DAB stage. Compared with the previous methods [20]-[22] the proposed technique have the following features: (1) The paper investigates the application of the SST converter in FREEDM system and its control with power flowing from the distributed renewable energy resources to the grid under unbalanced conditions. (2) The DAB stage is used to boost the low input voltage of renewable energy sources to medium voltage level of the ac grid distribution. Therefore, multiple renewable energy sources can be used in parallel to increase the power rating of the system. (3) The dc-link voltage drift is controlled by two independent controllers. The DAB master-slave and the additional feedforward voltage balance mechanism embedded in the CHMI modulation stage. (4) It simplifies the controller of the DAB stages using master-slave method and provides high frequency galvanic isolation between the input and output.

This paper is organized as follows: the modeling of the SST including DAB converter and cascaded H-bridge multilevel inverter is discussed in Section II. Section III presents the proposed control method to resolve the issues of power and voltage unbalance and gives the corresponding simulation to verify the control algorithm. Section IV shows experiments results based on a scaled-down prototype of the SST, and Section V gives the conclusions.

## II. THREE-PHASE SST MODELING AND CONTROL

The topology and control strategy of three-phase SST (Fig. 2) are developed in this section. The prototype of the SST is rated as input dc-link voltage of 400V, output ac-voltage of 10kV and output power of 20kVA. The first stage of SST is high-frequency DAB converter which boosts low-voltage dc input to high-voltage dc link. The second stage is CHMI, which converts the dc link voltage to medium voltage ac grid, and controls active and reactive power delivered to grid.

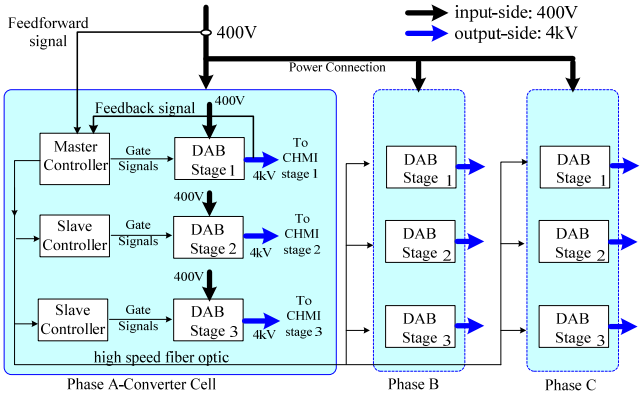


Fig. 3. Master-slave control diagram of the DAB converter stages.

Fig. 3 shows architecture of the DAB stages and their control circuit. The DAB stage steps up the 400V dc input to 4kV dc output which is fed to CHMI stage. In the proposed control circuit only one DAB converter is utilized as the master PI (proportional-Integral) voltage controller, which executes all control and modulation calculations and sends the resultant converter driving command signals to other DAB slave controllers via high speed fiber optic. Typically, DAB slave controllers only manage devices switching and protection. Also to calculate the power transferred by each module and implement the protection of over-voltage and over-current, the voltage and current of input-side and output-side are all sensed. Since circuit structure is completely identical, the output voltage amplitude of each DAB converter should be equal to the reference voltage with the same driving signals assuming that the components (switches and transformers) of each DAB stage are ideal. However, it is unlikely to have 100% identical switching devices and transformer parameters for each DAB, resulting in slightly unbalanced of power transferred by DAB modules. Nevertheless, this unbalanced can be also compensated by the CHMI controller stage which will be discussed in Section III. Therefore, the proposed master-slave controller in the DAB stage not only provides the high frequency galvanic isolation, but also simplifies the complex algorithm and improves the dynamic performance.

The function of CHMI stage is to produce sinusoidal 3-phase output voltage/current and control the active/reactive power injected into the grid. Fig. 4 shows the block diagram of 3-phase decoupled current controller developed for the CHMI stage.

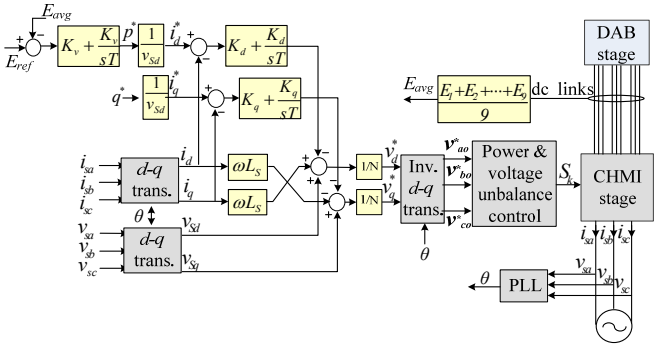


Fig. 4. Control scheme of the three-phase grid currents.

The average of all the dc link voltages is used to determine command of the total real power references $P^*$ needed to control the output of the three-phase system.The controller of CHMI stage in Fig. 4 contains two loops (1) outer voltage loop and (2) inner current loop. The outer voltage loop regulates the average dc-link voltages in order to determine the overall active power P needed to control the system. The distribution of that active power among different modules is later compensated in the modulation stage of the power balancing (per-phase Fig. 9) and (per-module Fig. 11). Therefore, the dc-link voltage drift is indirectly dealt with by modulating the voltage reference amplitude of each phase according to the respective imbalance proportion which causes unbalanced power drawn by each module until the balance is achieved. In addition, the reactive power reference can be controlled at different values depending on the system requirements. According to the three-phase $d$-$q$ transformation, the ac-voltage commands ($v_d^*$ and $v_q^*$) in the $d$-axis and $q$-axis is expressed by

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \frac{1}{N}\left( \begin{bmatrix} v_{Sd} \\ 0 \end{bmatrix} - \begin{bmatrix} 0 & -\omega L_{AC} \\ \omega L_{AC} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - K_P \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} - K_I \int \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} dt \right) \quad (1)$$

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where $i_d$ is the $d$-axis current, $i_q$ is the $q$-axis current, $i_d^*$ is the $d$-axis current reference, $i_q^*$ is the $q$-axis current reference, $\omega$ is the frequency of rotation of the reference frame in rad/sec, $v_{Sd}$ is the $d$-axis component corresponding to the three-phase grid voltage, and $L_{AC}$ is the ac line inductor. Note that the coefficient 1/N in Fig. 4 represents the number of cascaded converters, which is $N = 3$ in this case. The command voltages are transformed back to the three-phase reference signals $v_{ao}^*$, $v_{bo}^*$ and $v_{co}^*$ by applying the inverse $d$-$q$ transformation, where they will be used as the PS-PWM modulator signals in CHMI stage. Then, equation (1) can be rearranged as

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L_{AC}}\begin{bmatrix} K_P(i_d^* - i_d) + K_I\int(i_d^* - i_d)dt \\ K_P(i_q^* - i_q) + K_I\int(i_q^* - i_q)dt \end{bmatrix} \quad (2)$$

Equation (2) signifies that $i_d$ and $i_q$ can be controlled independently from each other, which means that the SST can provide active and reactive power control for the 10kV-ac grid independently. Meanwhile, in order to properly address the inherent power and voltage unbalance issues due to the difference of module parameters, an additional control strategy is added into the modulation stage, which is the second focus of this research.

Due to the modularity of topology, Phase-Shifted PWM (PS-PWM) is the optimum modulation method for CHMI stage. The switching state of one H-bridge-module $S_k$ is determined by the logical value of two signals ($S_{k1}$, $S_{k2}$), which can be "1" and "0" representing the "ON" and "OFF" state of each switch, respectively. This leads to four different binary combinations that generate three different output voltage $+V_{dc}$, $0$, and $-V_{dc}$. Since these H-bridge-modules are connected in series, the total output voltage of one phase $m$ ($m$=a, b, c) is given by

$$v_{mN} = \sum_{y=1}^{k} v_{my} = \sum_{y=1}^{k} V_{dc}(S_{y1} - S_{y2}) \quad (3)$$

Where k is the number of power modules per phase and $V_{dc}$ is the dc-link voltage of each module. The series connection of $k$ modules will produce $2k$+1 voltage levels in the total converter output voltage.

The PS-PWM modulation principle with 3 modules per phase is shown in Fig. 5. Due to the modularity of the topology, each module can be modulated independently using unipolar PWM with the same reference signal [25]. In this paper, three modules carrier signals are controlled at the same frequency 1 kHz and shifted by $2\pi/3$ rad from each other. Since the phase shift introduces a multiplicative effect, the CMHI line-to-neutral voltage has a switching pattern with 3 times the frequency the switching devices of each module. Hence, this converter can easily reach medium-voltage without the low frequency transformer and the total harmonic distortion (THD) is lower.

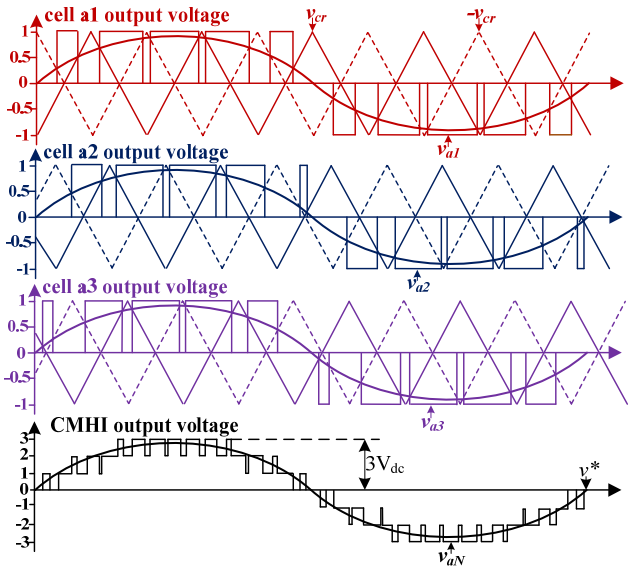


Fig. 5. Phase-shifted PWM waveforms for a 3-module CHMI.

Fig. 6 shows the digital control architecture of the CHMI based on DSP and FPGA. The sampled data consists of dc-high-side voltage/current and three-phase grid voltage/current. The synchronization of the $d$-$q$ transformation is performed through a phase-locked loop (PLL) to regulate the active and reactive power in the DSP controller. Meanwhile, the power and voltage unbalance compensation calculation have also been added into the controller. Since the frequency of the switching devices of each module is 1 kHz, the sampling frequency is 6 kHz and the reference update period is 1ms. Therefore, the digital control system has to execute a sequence of voltage/current signal acquisition and voltage reference computation within the sampling period of 167 μs (1s/6k). The DSP sends voltage references every 167 μs to FPGA, which plays an essential role in using phase-shifted clock to generate 36 corresponding PWM signals. The problem description and solution of the inherent unbalance among three phases and different modules of one phase is discussed in the next section.

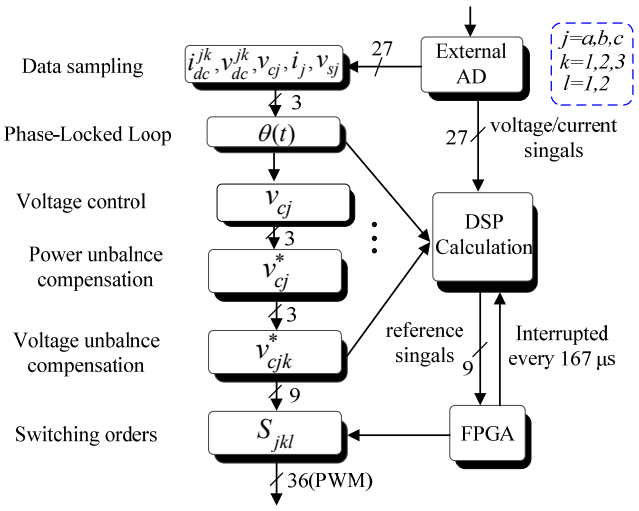


Fig. 6. Software block diagram for the CHMI stage.

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## III. Power and Voltage Balance Control Scheme

Since sending the same PWM signals to each DAB by fiber optic, the power is evenly distributed among the modules. However, this is unlikely to have identical switching devices and high-frequency transformer parameter for each DAB, resulting in the difference of power transferred by DAB modules. Consequently, this situation originates two types of imbalance in CHMI stage: per-phase and per-module. The first unbalance problem is the difference of real power delivered by each phase ($P_a \neq P_b \neq P_c$), while the second is the difference of real power delivered by each module of phase $m$ ($P_{m1} \neq P_{m2} \neq P_{m3}$). These two unbalances affect the performance of the CHMI in two different ways: the per-phase unbalance affects the current inner-loop leading to unbalanced grid currents which generates a power pulsation in the output ac-side. The per-module unbalance will make the dc-link voltage drift from its reference value, result in distortion and potentially damaging power devices by overvoltage. In this section, these two types of unbalance will be addressed.

### *A. Per-phase Power Unbalance Compensation Scheme*

The objective of this control approach is to share equally the power at the 3-phase ac-side under unbalance conditions. In order to present the scheme, assume that the power transferred by DAB of phase A is lower than phase B. As shown in Fig. 2, the line-to-neutral voltage equation of the power circuit can be described by

$$\begin{cases} v_{sa} = v_{ao} - L\dfrac{di_{sa}}{dt} - Ri_{sa} + u_{NO} \\ v_{sb} = v_{bo} - L\dfrac{di_{sb}}{dt} - Ri_{sb} + u_{NO} \\ v_{sc} = v_{co} - L\dfrac{di_{sc}}{dt} - Ri_{sc} + u_{NO} \end{cases} \quad (4)$$

For a star-connection cascade inverter the neutral point is floating, since it is not grounded. Thus, it is difficult for current controller to directly produce the 3-phase reference voltages to maintain the balanced output currents under unbalanced conditions. Note that the common voltage $u_{NO}$ can affect the 3-phase currents according to equation (4).

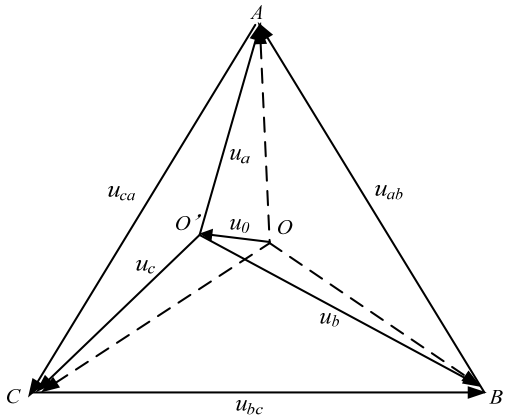


Fig. 7. Phasor voltage with the proposed neutral point shift method.

This is an important characteristic because it shows that is possible to rebalance 3-phase currents by moving the neutral point "*O*" to change the respective reference voltage. In addition, the neutral point will be moved through an optimum zero sequence injection.

Fig. 7 shows an example of voltage phasor triangle to rebalance 3-phase currents under unbalanced conditions. When the power transferred by 3-phase modules is the same, the output line-to-neutral voltage amplitudes of each phase are equal as shown by dotted lines. Assume the power transferred by phase A is less than the others, if the reference output voltage of each phase is still the same, the output current of phase A will be lower. As a result, unbalanced output current occurs and causes failure for the grid connection. Therefore, to maintain balanced three-phase currents this paper employs the moving floating neutral point algorithm to produce different output voltage reference for each phase. Note that the line-to-line voltages remain unchanged as shown in Fig. 7, meaning that the injection of zero-sequence voltage phasor $U_0$ will not alter the sum of three-phase active powers.

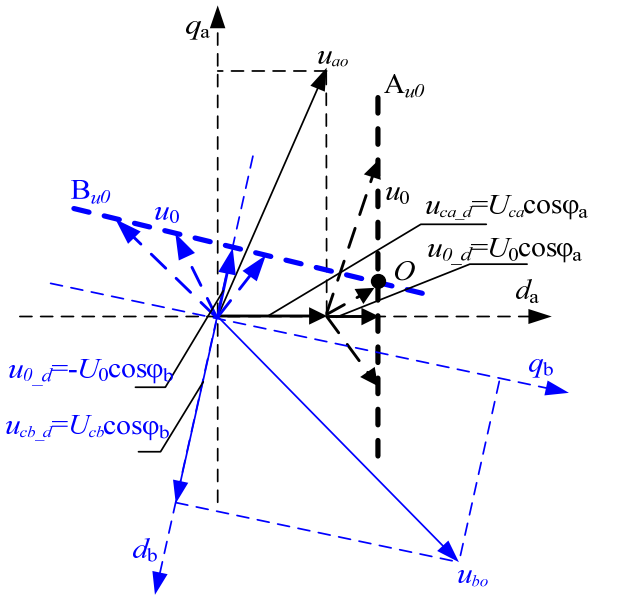


Fig. 8. Phasor diagram showing how to find out zero-sequence voltage $U_0$.

The next task is finding the zero-sequence component $U_0$. The zero sequence is regulated according to the deviation of the power transferred by each phase from the average power. Therefore, first determine the total active power transferred by the three-phase DAB modules. If the DAB converters of each phase are delivering $P_m (m = a, b, c)$ to the corresponding cascaded H-bridge, when the system is considered lossless, the summed active power delivered to the grid is $P_\Sigma = P_a + P_b + P_c$, and each phase should provide $P_{av} = P_\Sigma/3$. Thus, under unbalanced conditions the active power in each phase should be controlled to the target value $P_{av}$. In order to achieve this condition, an unbalance ratio $r_m$ is calculated as $r_m = P_{av}/P_m$. In the unbalanced case, if $P_{av} > P_m$ the unbalance ratio is larger than 1 and the injected zero sequence allows to this phase increases its currents. On the other hand if $P_{av} < P_m$, its unbalance ratio is lower than 1 and the zero sequence reduces the corresponding current.

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Then, adjust the active power in each phase to the target value using the zero-sequence voltage $U_0$. As illustrated in Fig. 8, the direct component of the voltage phasor contributes to the generation of active power. Note that the amplitude of the direct component of $U_{ca}$ is $U_{ca}\cos\varphi_a$, to increase active power from $P_a$ to $P_{av}$ in phase A, the necessary and sufficient condition is that the voltage phasor $U_0$ should be located on the line $A_{u0}$. In the same way, the necessary and sufficient condition for reducing active power from $P_b$ to $P_{av}$ in phase B is that the phasor $U_0$ is located on the line $B_{u0}$. Consequently, to guarantee $P_{av}$ in both phase A and B, the resultant phasor $U_0$ must be located at the intersection of these two lines. In addition, when the average active power in phase A and phase B have been controlled to be $P_{av}$ simultaneously, the active power in phase C is naturally $P_{av}$ as well. The mathematical proof is presented as follow.

First, calculate the amplitude and phasor of injection of zero sequence voltage $U_0$. The average active power in each phase can be expressed by

$$\begin{cases} \frac{1}{2}U_{ao}I_a\cos(\varphi_{ao}-\varphi_{ia})+\frac{1}{2}U_0I_a\cos(\varphi_0-\varphi_{ia})=\mathrm{P}_a+\mathrm{P}_0=\mathrm{P}_{av} \\ \frac{1}{2}U_{bo}I_b\cos(\varphi_{bo}-\varphi_{ib})-\frac{1}{2}U_0I_b\cos(\varphi_0-\varphi_{ib})=\mathrm{P}_b-\mathrm{P}_0=\mathrm{P}_{av} \end{cases} \tag{5}$$

The equation (5) can be rewritten as

$$\begin{cases} \frac{1}{2}U_0I_a\cos(\varphi_0-\varphi_{ia})=\mathrm{P}_{av}-\mathrm{P}_a=\mathrm{P}_a(\mathrm{r}_a-1) \\ \frac{1}{2}U_0I_b\cos(\varphi_0-\varphi_{ib})=\mathrm{P}_b-\mathrm{P}_{av}=\mathrm{P}_b(1-\mathrm{r}_b) \end{cases} \tag{6}$$

By separately dividing the left and the right parts of (6) by each other, a factor can be obtained by

$$k_{\mathrm{com}}=\frac{\cos(\varphi_0-\varphi_{ia})}{\cos(\varphi_0-\varphi_{ib})}=\frac{I_b}{I_a} \tag{7}$$

$$k_{\mathrm{com}}=\frac{U_{ao}\cos(\varphi_{ao}-\varphi_{ia})(\mathrm{r}_a-1)}{U_{bo}\cos(\varphi_{bo}-\varphi_{ib})(1-\mathrm{r}_b)} \tag{8}$$

Substituting the obtained $k_{\mathrm{com}}$ from (8) into (7)

$$\frac{\cos(\varphi_0-\varphi_{ia})}{\cos(\varphi_0-\varphi_{ib})}=\frac{U_{ao}\cos(\varphi_{ao}-\varphi_{ia})(\mathrm{r}_a-1)}{U_{bo}\cos(\varphi_{bo}-\varphi_{ib})(1-\mathrm{r}_b)} \tag{9}$$

Then, a solution of the phase of $U_0$ can be obtained by

$$\varphi_0=\tan^{-1}\frac{\cos\varphi_{ao}-k_{com}\cos\varphi_{ib}}{k_{com}\sin\varphi_{ib}-\sin\cos\varphi_{ao}} \tag{10}$$

Finally, substituting the calculated into (5), the zero sequence of $U_0$ can be obtained by using the known voltage and current parameters

$$U_{0m}=\left|\frac{2P_ar_a-U_{ao}I_a\cos(\varphi_{ao}-\varphi_{ia})}{I_a\cos(\tan^{-1}(\frac{\cos\varphi_{ao}-k_{com}\cos\varphi_{ib}}{k_{com}\sin\varphi_{ib}-\sin\cos\varphi_{ao}})-\varphi_{ia})}\right| \tag{11}$$

After obtaining the zero sequence voltage $U_0$ is calculated according to (11), and injecting to each reference to introduce the corresponding line-to-neutral voltage shift. This originates the compensated phase voltage reference is given in the Fig. 9.

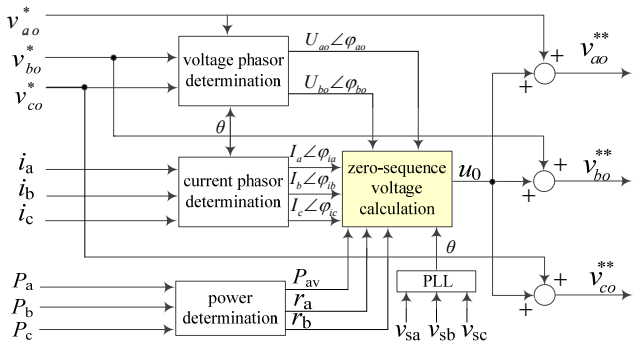


Fig. 9. Block diagram of the proposed per-phase power balance controller.

Then, prove that the zero-sequence voltage $U_0$ cannot change the three-phase summed active and reactive power. The summed three-phase active power without the zero sequence injection can be expressed by

$$\frac{1}{2}U_{ca}I_a\cos(\varphi_{ca}-\varphi_{ia})+\frac{1}{2}U_{cb}I_b\cos(\varphi_{cb}-\varphi_{ib})+\frac{1}{2}U_{cc}I_c\cos(\varphi_{cc}-\varphi_{ic})=P_\Sigma \tag{12}$$

Note that $i_a+i_b+i_c=0$ at the neutral point for the star-connected converter, thus the three-phase power generated by zero sequence voltage $u_0$ will be zero as expressed by

$$p_0=u_0i_a+u_0i_b+u_0i_c=0 \tag{13}$$

Then, the summed three-phase active power generated by voltage $u_0$ can be expressed by

$$\frac{1}{2}U_0I_a\cos(\varphi_0-\varphi_{ia})+\frac{1}{2}U_0I_b\cos(\varphi_0-\varphi_{ib})+\frac{1}{2}U_0I_c\cos(\varphi_0-\varphi_{ic})=0 \tag{14}$$

Due to $P_\Sigma=P_a+P_b+P_c=3P_{av}$, the active power of phase A and phase B have been adjusted to $P_{av}$, simultaneously. By adding (12) and (14), the average power in phase C can be obtained by

$$\frac{1}{2}U_0I_c\cos(\varphi_0-\varphi_{ic})+\frac{1}{2}U_{cc}I_c\cos(\varphi_0-\varphi_{ic})=P_\Sigma-P_a+P_b=P_c \tag{15}$$

Therefore, provided that the average active power in phases A and B has been controlled to be $P_{av}$, using the calculated $U_0$, the average active power in phase C is naturally $P_{av}$ as well.

### *B. Per-Module Voltage Unbalance Control Mechanism*

Since each phase consists of three DAB dc/dc converters, the power unbalanced can appear on the different modules of one phase due to the device loss mismatching and H-Bridge active power differences. The dc link voltage drift must be avoided, because this unbalanced situation might cause the capacitor or IGBT device overvoltage and trigger the system overvoltage protection.

To overcome the problem, the phase voltage reference ($v_{ao}^{**}$, $v_{bo}^{**}$, $v_{co}^{**}$) of the CHMI controller is modulated using a feedforward control loop that takes into account the voltage drift in the dc-link of each module. The balanced mechanism is

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to modulate the voltage reference amplitude of each phase according to the respective unbalance proportion and this leads to different power drawn by each module until the balance is achieved. Ultimately, the dc-link voltage can be balanced as the power drawn is balanced. Note that the feedforward control loop has a slower response compared to the three phase balancing mechanism.

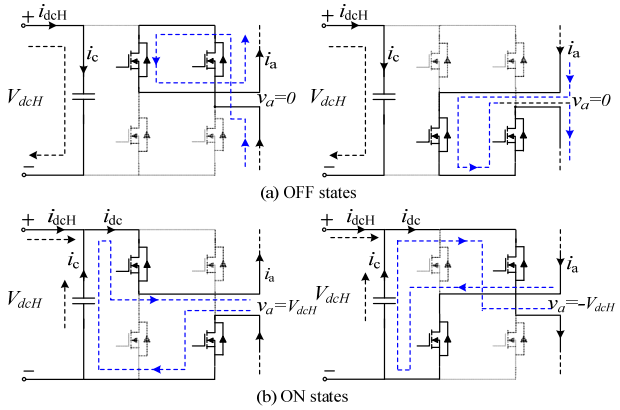


Fig. 10. Per cell dc-link voltage dependence on the switching states of for one H-bridge module.

To better understand the modulation, the different switching states of one module are shown as Fig. 10. It can be seen that the OFF states isolates the dc-link capacitor from the converter. Hence the module current $i_{\mathrm{dcH}}$ is equal to the capacitor current $i_{\mathrm{c}}$ charging the capacitor, increasing the dc-link voltage $V_{\mathrm{dcH}}$. On the contrary during the ON-states, when generating $+V_{\mathrm{dcH}}$ or $-V_{\mathrm{dcH}}$ on the positive cycle and negative cycle, the capacitor current $i_{\mathrm{c}}$ is equal to $i_{\mathrm{dcH}}$-$i_{\mathrm{dc}}$, thus reducing the voltage $V_{\mathrm{dcH}}$.

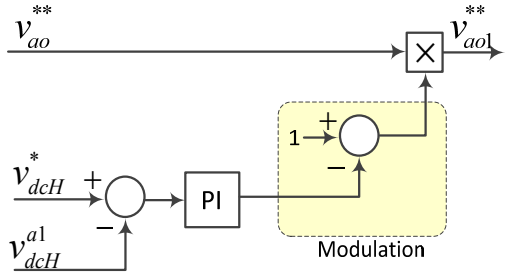


Fig. 11. Per-module dc-link voltage balance controller (feedforward compensation).

Fig. 11 shows the voltage balance example based on the module #1 of phase A. The dc-link voltage error $(v^{*}_{\mathrm{dcH}} - v^{\mathrm{a1}}_{\mathrm{dcH}})$ is controlled by a PI controller, whose output is used to adjust the amplitude of each module voltage reference. In the way, the amplitude of line-to-neutral voltage reference of each module is modified proportionally to the error of their respective dc-link voltages. This result in a feedforward correction redistributes the ON and OFF times so that the voltage balance is achieved.

### C. *Analysis of Stability Operation Range*

Due to the intrinsic constraints of the cascaded H-bridge structure, there is a limitation on the degree of unbalance in practical applications [22]. According to the principle of the compensation scheme, this might result in over modulation when the power transferred by DAB module is strongly unbalanced. If the power unbalance is out of the derived range, this controller will not be able to balance the dc-link voltages and 3-phase current. To better understand of the stability margin, the paper utilizes mathematical model to analyze the converter operation. In the steady state, according to Fig. 2 the voltage of Phase A can be described as follow:

$$\begin{cases} v_{ao} = v_{sa} + j\omega L i_{sa} - u_{NO} \\ v_{sn} = v_{ao} + u_{NO} \\ v_{sn} = v_{sa} + j\omega L i_{sa} \end{cases} \tag{16}$$

$$v_i = \left(m_{di} + jm_{qi}\right) E_{ref} \tag{17}$$

where $E_{ref}$ is the dc-link output voltage reference of DAB module, $v_i$ is the ac-side output voltage of $i$th H-bridge, $i_{sa}$ is the output ac current and $m_{di}$ and $m_{qi}$ are the modulation index of the direct and orthogonal components of the associated module, respectively. Then, the output voltage of cascade inverter $v_{sn}$ can be rearranged as:

$$v_{sn} = \sum_{1}^{i=N} v_i = \sum_{1}^{i=N} \left(m_{di} + jm_{qi}\right) E_{ref} = v_{sa} + j\omega L i_{sa} \tag{18}$$

where $N$ is the number of cascaded H-bridge and the modulation index of d-q axis can be deduced as:

$$\sum_{1}^{i=N} m_{di} = \frac{v_{sa}}{E_{ref}}, \quad \sum_{1}^{i=N} m_{qi} = \frac{\omega L i_{sa}}{E_{ref}} \tag{19}$$

The total injected to the grid active and reactive power is:

$$\sum_{1}^{i=N} P_i + jQ_i = i_{sa} \sum_{1}^{i=N} v_i = i_{sa} \sum_{1}^{i=N} \left(m_{di} + jm_{qi}\right) E_{ref} \tag{20}$$

Assume, the reactive power is equally distributed, so $m_{qi} = \dfrac{\omega L i_{sa}}{N E_{ref}}$. If the controller is stable, $m_{di}^2 + m_{qi}^2 \le 1$. Then:

$$m_{di} \le \sqrt{1 - \left(\frac{\omega L i_{sa}}{N E_{ref}}\right)^2} \tag{21}$$

Based on the ac-side output current $i_{sa} = \dfrac{P_{\Sigma}}{v_{sa}}$, so the $i$th module power can be described:

$$P_i = i_{sa} m_{di} E_{ref} = \frac{P_{\Sigma} m_{di} E_{ref}}{v_{sa}} \tag{22}$$

The $m_{di}$ is derived as:

$$m_{di} = \frac{v_{sa} P_i}{P_{\Sigma} E_{ref}} \tag{23}$$

The maximum modulation index of the direct can be described:

$$m_{\mathrm{d\,max}} = \max\left\{m_{d1}, \mathrm{m}_{d2} \ldots \mathrm{m}_{dN}\right\} \tag{24}$$

$$m_{\mathrm{d\,max}} = \frac{v_{sa} P_{\max}}{P_{\Sigma} E_{ref}} \le \sqrt{1 - \left(\frac{\omega L i_{sa}}{N E_{ref}}\right)^2} \tag{25}$$

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Substitute $m_{dmax}$ with the equation (23), then the maximum power $P_{\max}$ should be meet the

$$\frac{P_{\max}}{P_{\Sigma}} \le \frac{E_{ref}}{v_{sa}} \sqrt{1-(\frac{\omega L i_{sa}}{N E_{ref}})^2} \tag{26}$$

Hence, according to the equation (26) the stability range of the system is derived, and the stability margin is determined by: the output ac voltage, dc link voltages reference, output inductance, and the number of H-bridges. So the proposed controller is indispensable to maintain the power unbalance within the stability range, so that the converter can stably operate.

*D.Simulation*

To verify the proposed power and voltage balance controller simulation prototype of Fig. 2 is implemented using Matlab/Simulink. The simulation parameters are listed in Table I.

TABLE I CIRCUIT PARAMETERSOF THE SIMULATION SYSTEM

| Basic Parameters | Symbol | Value |
|---|---|---|
| Output AC Voltage | $V_S$ | 10kV |
| Power Rating | $P$ | 20kVA |
| Cascaded Number | $N$ | 3 |
| AC-Side Inductance | $L_{AC}$ | 2mH |
| AC-Side Resistance | $R_S$ | 0.1mΩ |
| Switching Device Frequency | $f$ | 500Hz |
| DC-Link Capacitance | $C$ | 5mF |
| Current Loop Control Parameters | $P$、$I$ | 0.5、0.2 |
| Voltage Loop Control Parameters | $P$、$I$ | 0.1、0.1 |

Since the DAB converter is a current source converter, the PV module with different P-V curves are utilized as the power supplied for each H-bridge of cascade inverter stage of SST in the simulation, emulating different power transferred by the DAB modules due to the mismatch in various parameters. In order to verify the proposed balance controller, the power levels of PV modules are changed two times, to emulate a phase unbalance and module unbalance.

The PV module curves corresponding to different power levels are shown in Fig. 12. First, all power modules of the CHMI start at the same power level $P_A$=$P_B$=$P_C$=1.0p.u. (P&V curve-I). Then at $t$=1s the PV modules power connected to the three modules of phase A are reduced to 0.9p.u. ($P_{A1}$=$P_{A2}$=$P_{A3}$=0.9p.u. P&V curve-II), simultaneously, forcing a phase unbalance. Further on, a step change is performed to module-B1and module-B2 at $t$=1.5s, which are decreased separately to 0.8p.u. and 0.9p.u. ($P_{B1}$=0.8p.u. P&V curve-III and $P_{B2}$=0.9p.u. P&V curve-II), and $P_{B3}$=1.0p.u. (P&V curve-I) forcing a module unbalance. Phase C is not modified throughout the operation. The simulation results for the dynamic and steady state performance are illustrated in Fig. 13-15.

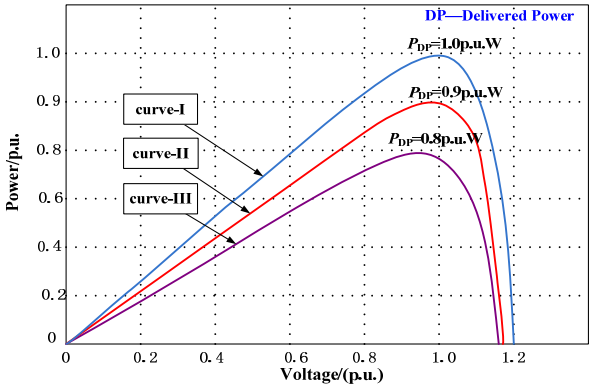


Fig. 12. Power versus voltage curves of PV module.

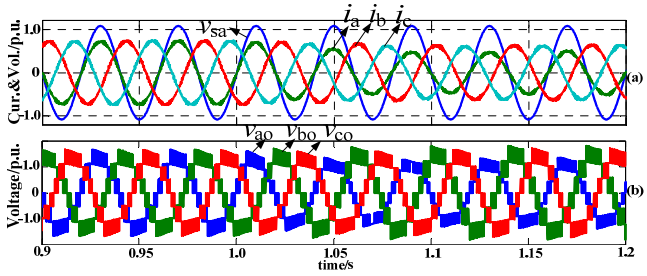


Fig. 13. Dynamic performance without power balance control. (a) Grid currents ($i_a$, $i_b$, $i_c$) and the grid voltage $v_{sa}$. (b) Three-phase line-to-neutral voltages ($v_{ca}$, $v_{cb}$, $v_{cc}$).

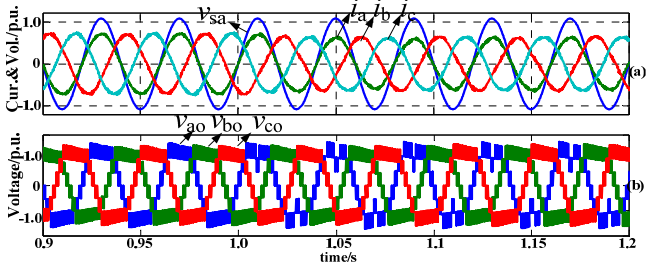


Fig. 14. Dynamic performance with power balance control. (a) Grid currents ($i_a$, $i_b$, $i_c$) and grid voltage $v_{sa}$. (b) Three-phase line-to-neutral voltages ($v_{ca}$, $v_{cb}$, $v_{cc}$).

Fig. 13 shows the dynamic performance of 3-phase output currents with a step phase unbalance in phase A at $t$=1s and no power balance control. The 3-phase delivered currents to the grid are unbalanced and the line-to-neutral voltage in phase A also becomes distorted. Meanwhile, the unbalanced condition also results in a pulsating power at the gird side, because the active power and reactive power are respectively proportional to the $d$-$q$ synchronous frame components of the grid current $i_{sd}$ and $i_{sq}$. Fig. 14 shows 3-phase output currents with the power balance control. With the power balance control, 3-phase grid currents are completely balanced despite the modules are operating at different power levels. This is because the injection of zero sequence voltage does not affect the line-to-line voltage.

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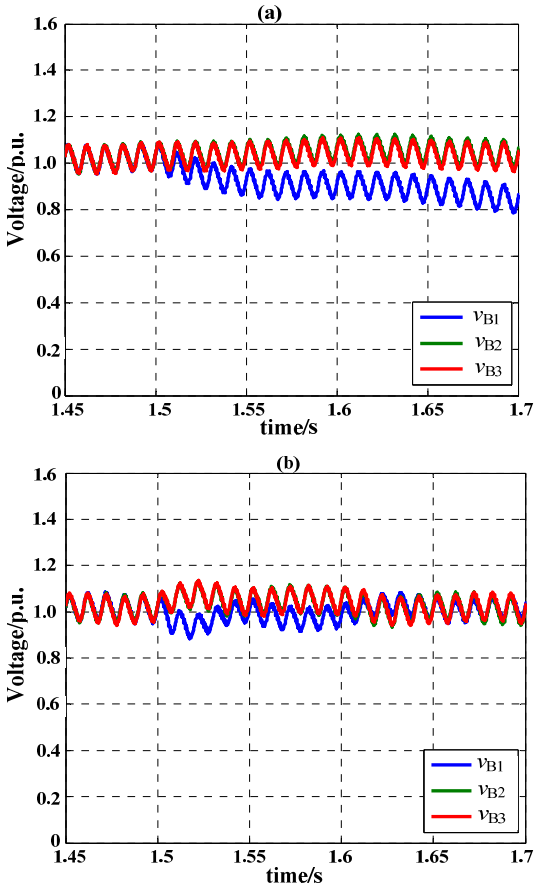


Fig. 15. Dynamic performance of three DC-link voltages of phase B. (a) Without voltage balance control. (b) With voltage balance control.

To validate the voltage balance control, the dc-link voltages of three modules of phase B are given in Fig. 15. Fig. 15(a) shows the three dc-link voltages cannot maintain at the reference value without voltage unbalance control. The reason is that the CHMI modulation stage imposes the same voltage reference for each module, while, their voltages drift when power transferred are different by DAB modules. The module that delivers more power has higher dc-link voltage. Fig. 15(b) shows the three dc-link voltages of phase B with the proposed voltage balance control. The output voltage values of the three modules are equal based on the voltage balance control. The controller modifies the amplitude of each module voltage reference according to their respective unbalance deviation, to redistribute the switching devices ON/OFF times. This reduction on the voltage reference causes a reduction on the ON time of the module for making a rise on the corresponding dc-link voltage.

## IV. Experimental Verification

To verify the performance of the three-phase system and the proposed power and voltage balance control scheme, a scaled-down prototype of three modules of each phase cascaded circuit is implemented. Fig.16 shows the experimental platform with output voltage 400V-ac, frequency 50Hz and rated power 10kVA. In the experiment, nine solar array simulators (SAS-Agilent E4350B) are utilized as the power supply of each module of CHMI, to emulate the difference of power transferred in the DAB stage, and whose power curve can be controlled to allow the emulation of step power changes. The SST control algorithms are programmed in DSP-TMS320F28335 and FPGA-A3P1000. The design parameters of the experiment are listed in Table II.

TABLE II Circuit Parameters of the Experiment System

| Basic Parameters | Symbol | Value |
|---|---|---|
| Output AC Voltage | $V_S$ | 400V |
| Power Rating | $P$ | 10kVA |
| Ratio of Output Star-Step-up Transformer | $n$ | 4 |
| Cascaded Number | $N$ | 3 |
| AC-Side Inductance | $L_{AC}$ | 2mH |
| Switching Device Frequency | $f$ | 1kHz |
| High Voltage DC Reference for Each Module | $V_C$ | 80V |
| DC-Link Capacitance | $C$ | 2mF |
| Open Circuit Voltage of Module | $V_{OC}$ | 100V |
| Short Circuit Current of Module | $I_{SC}$ | 5A |

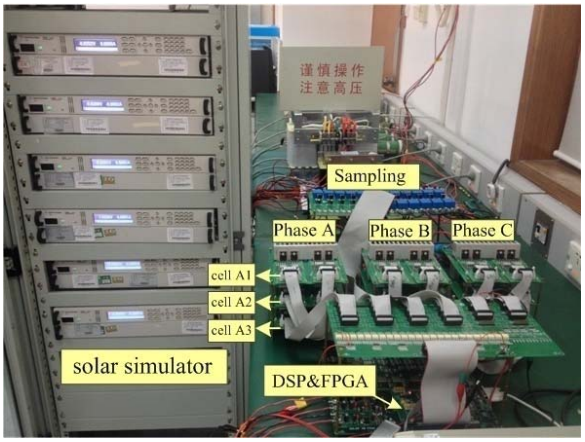


Fig. 16. Experimental platform of the three-phase system.

In the experiment, the same power curves (corresponding to the curve-I of Fig. 12) are programmed in the nine solar array simulators, the active power reference is set to $P^*$=5kW and the reactive power is set to zero. The line-to-neutral voltage $V_{AN}$, $V_{BN}$, $V_{CN}$ and line-to-line voltage $V_{AB}$ are shown in Fig. 17. There are five levels at each phase and nine levels at line-to-line, and the number of output voltage levels is proportional to the amplitude of active power reference. Fig. 18 shows the output ac-side voltage in phase A and 3-phase currents. As can be seen, the idea sinusoidal waveforms are produced, and low harmonics will bring a significant reduction in switching power loss.

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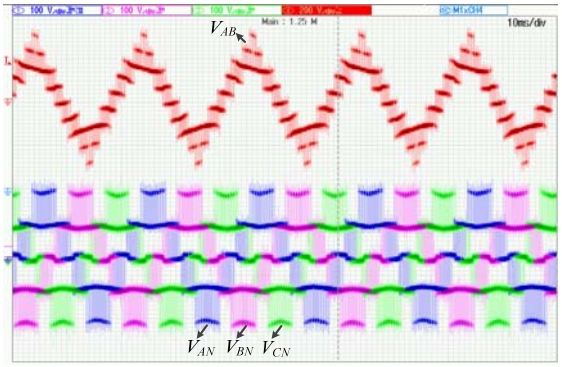



Fig. 17. Experiment results of three-phase CHMI stage. (Ch1, output voltage of line-to-line $V_{AB}$, 200V/div; Ch2, output line-to-neutral voltage of phase A $V_{AN}$, 100V/div; Ch3, output voltage of phase B $V_{BN}$, 100V/div; Ch2, output voltage of phase C $V_{CN}$, 100V/div).

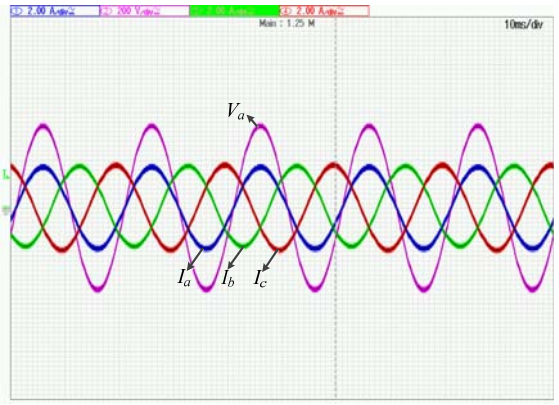
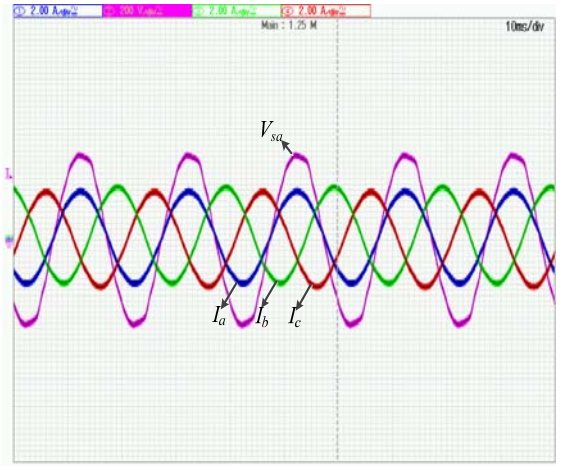
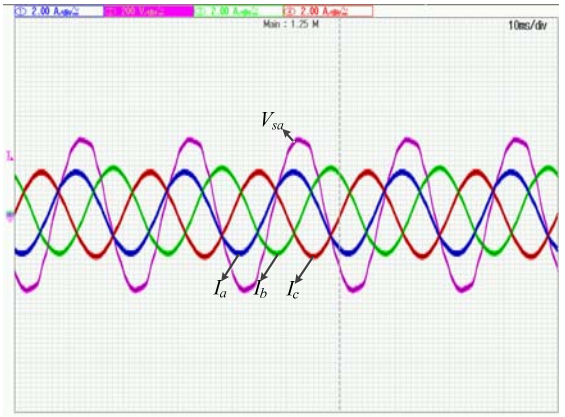


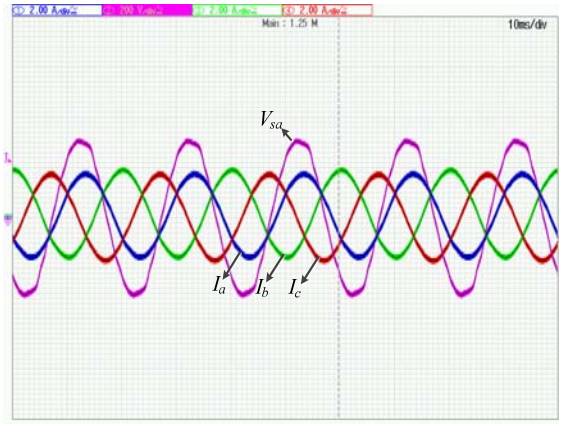

Fig. 18. Output performance of three-phase CHMI. (Ch1, output current of phase-A $I_a$, 2A/div; Ch2, output grid-side voltage of phase A $V_a$, 200V/div; Ch3, output current of phase B $I_b$, 2A/div; Ch4, output current of phase C $I_c$, 2A/div).




(a)




(b)




(c)

Fig. 19. Experiment results of reactive power control. (Ch1, output current of phase A $I_a$, 2A/div; Ch2, the grid voltage of phase A $V_{sa}$, 200V/div; Ch3, output current of phase B $I_b$, 2A/div; Ch4, output current of phase C $I_c$, 2A/div). (a) Reactive-power reference $Q^*$=0. (b) Reactive-power reference $Q^*$>0. (c) Reactive-power reference $Q^*$<0.

Fig. 19(a) demonstrates the steady-state experiment results of the three-phase CHMI stage, whose reactive power reference is set to zero. Note that the output phase A current is completely in phase with the corresponding grid voltage, which means a unity power factor. The three-phase CHMI not only regulates the active power to the grid, but also has reactive power compensation capabilities. The SST can generate or absorb reactive power to the grid through controlling the reactive power reference. As shown in Fig. 19(b), the output current is leading the grid voltage, so the SST is generating reactive power to the grid. In Fig. 19(c) the output current is lagging the grid voltage, so the SST is absorbing reactive power from the grid.

In order to verify the proposed 3-phase power balance control, the power levels of the six solar array simulators connected to phase A and phase B are dynamically changed, to emulate the difference of active power transferred. In this experiment, the power versus voltage curves of phase A and Phase B are changed from curve-I to curve-II of Fig. 12, while phase C maintains as curve-I. Fig. 20(a) illustrates the system without the power balance control. The three-phase currents are balanced when the power transferred are equal. While the three-phase currents become unbalanced after the supply power change, it is not allowed to inject the unbalanced current into the grid. Fig. 20(b) shows the three-phase currents

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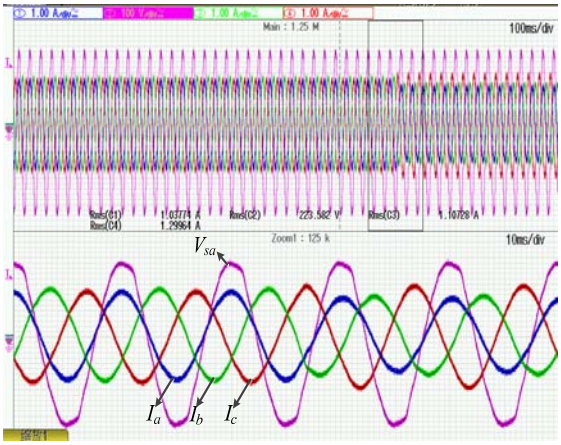
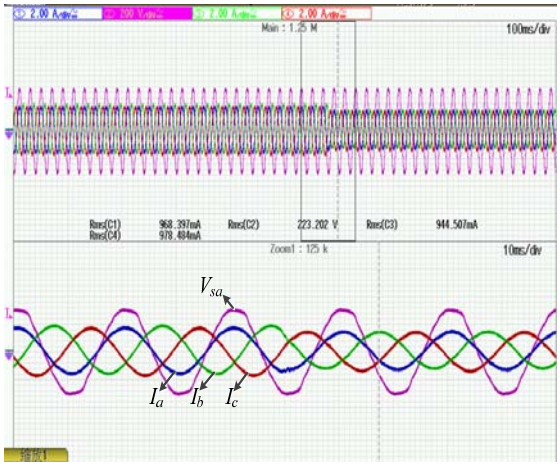
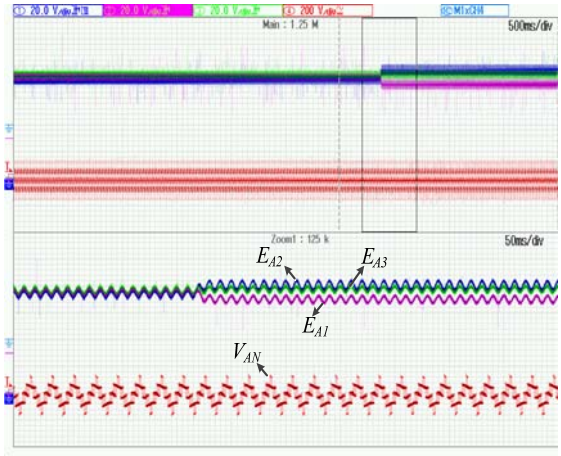



(a)

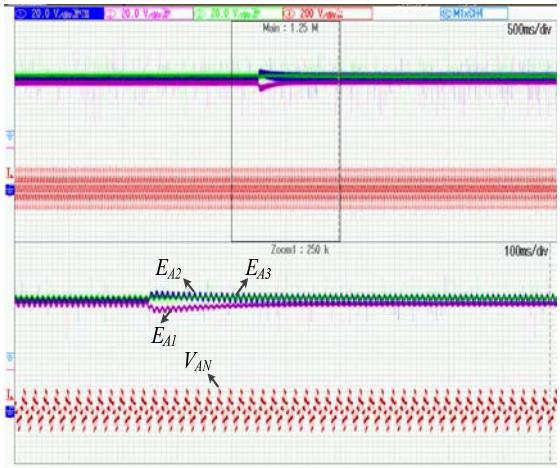



(b)

Fig. 20. Experiment results testing for the power control. (Ch1, output current of phase A $I_a$; Ch2, the grid voltage of phase A $V_{sa}$, 200V/div; Ch3, output current of phase B $I_b$; Ch4, output current of phase C $I_c$). (a) Three-phase output currents without power balance control. (b) Three-phase output currents with power balance control. (For clearly showing the unbalance, three-phase currents of Fig. 20(a) are regulated to 1A/div, Fig. 20(b) 2A/div).




(a)




(b)

Fig. 21. Experiment results testing for the voltage balance control. (Ch1, DC-link voltage of module-A1 $E_{A1}$, 20V/div; Ch2, DC-link voltage of module-A2 $E_{A2}$, 20V/div; Ch3, DC-link voltage of module-A3 $E_{A3}$, 20V/div; Ch4, phase A output voltage of multilevel $V_{AN}$, 200V/div). (a) DC-link voltage without voltage balance control. (b) DC-link voltage with voltage balance control.

are equally controlled with the proposed power balance control under unbalanced conditions. The experiment verifies the effectiveness of the proposed balance controller.

In order to further test the performance of voltage balance control, the three SAS connected to phase A as power supplied are programmed at different power levels to create a module unbalance. In this experiment, the dc-link voltage reference is set to $v_{dcH}^{*}$=80V, then the curve of module-A1 is changed from curve-I to curve-II of Fig. 12, and module-A2 and module-A3 maintain as curve-I. Fig. 21(a) illustrates the three dc-link voltages without the voltage balance control. First, the three dc-link voltages are all regulated at 80V under the same power curves of solar array simulators. However, after the module-A1 power level changes, the dc-link voltages become unbalance. The module with a larger power level has a higher dc-link voltage. Fig. 21(b) shows the three dc-link voltages are well regulates to the target value with the proposed voltage balance control.

## V. Conclusion

This paper proposes a novel control scheme of CHMI based on SST system for microgrid applications, operating under unbalanced conditions. The detailed control method is analyzed to address the presence of power and voltage unbalance: among three phases and the different modules of one phase. First, the line-to-neutral reference voltage of each phase is regulated through injection a zero sequence voltage to maintain the balanced three-phase grid currents. Then, the modulation index of each module is modified according to the difference of dc-link voltage, to dynamically regulate the dc-link voltage of each module to the target value. The proposed balance control strategy is characterized for producing high quality grid currents and reactive power compensation. In addition, a high speed fiber-optic is employed to send switching commands from a central master controller to other slave controllers in DAB stage, which leads to simplify complex control algorithm and improve system dynamic performance. Finally, the simulation and experiment

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results obtained from a 400V 10kVA laboratory downscaled model verify the proposed circuit and control scheme.

## APPENDIX

In this paper, the three-phase line-to-neutral voltages, output currents and zero-sequence voltage can be expressed in phasor forms as follows:

$$u_{ca}=U_{ca}\angle\varphi_{ca}, u_{cb}=U_{cb}\angle\varphi_{cb}, u_{cc}=U_{cc}\angle\varphi_{cc},$$

$$i_a=I_a\angle\varphi_{ia}, i_b=I_b\angle\varphi_{ib}, i_c=I_c\angle\varphi_{ic}, u_0=U_0\angle\varphi_0.$$

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